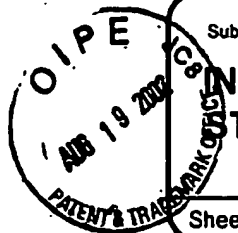


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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

### Complete if Known

Application Number	09/998,523
Filing Date	November 29, 2001
First Named Inventor	Vishal Sharma
Group Art Unit	2661
Examiner Name	na
Attorney Docket Number	04910000012

### OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials <sup>2</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
NN		IYER, Sundar et al.; Analysis of a packet switch with memories running slower than the line-rate; Computer Systems Laboratory, Stanford University	
NN		MNEIMNEH, Saadeddine S. et al.; On Scheduling Using Parallel Input-Output Queued Crossbar Switches With No Speedup; Massachusetts Institute of Technology and Jasmine Networks, Inc.; pages 1-17	
NN		CHANEY, Tom J. et al.; Design of a Gigabit ATM Switch; Washington University; February 5, 1996	
NN		KRISHNA, Pattabhiraman et al.; On the Speedup Required for Work-Conserving Crossbar Switches; IEEE Journal on Selected Areas in Communications; Vol. 17, No. 6, June 1999; pages 1057-1066	
NN		CHUANG, Shang-Tse; Matching Output Queueing with a Combined Input/Output-Queued Switch; IEEE Journal on Selected Areas in Communications; Vol. 17, No. 6, June 1999; pages 1030-1039	

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<sup>1</sup> Unique citation designation number. <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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Sheet 1 of 1

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**Examiner  
Signature**

Date Considered

6/21/2005

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